

REMARKS

Claims 15-22, as amended, remain herein. Claim 23 is newly added.

Applicants note and appreciate the indication of allowable subject matter in claims 16, 17, 18 and 20-22. Claims 15, 17 and 21 have been amended to correct informalities. Claim 15 has also been amended to recite "digital signals outputted from the A/D conversion means successively in a predetermined order, to generate a control signal for controlling the optical system," "setting beforehand the order of acquiring the digital signals which are outputted from the arithmetic process means," and "instructing to perform an A/D conversion according to the set acquisition order." Claims 16, 17 and 20 have been amended to include all of the limitations of the base claim and any intervening claims to place them in a condition for allowance.

This Amendment is believed to place this application fully in condition for allowance, and surely places it in better condition for any appeal. Thus, entry of this Amendment and allowance of all claims 15-23 are respectfully requested.

1. The claims have been amended for clarity by editing out the informalities noted in the Office Action.

2. Claim 18 has been amended as suggested in the Office Action to moot the rejection under 35 U.S.C. §112, paragraph 2.

3. Claims 15 and 19 were rejected under 35 U.S.C. §103(a) over Shio Japanese Patent Application Publication No. 06-236556 (JP '556) in view of Imamura et al U.S. Patent 4,287,802.

Claim 15, as presently amended, recites in part that:

an arithmetic processing means for performing arithmetic processing on the digital signals outputted from the A/D conversion means;

said A/D conversion command means for first setting an order of acquiring digital signals outputted from the arithmetic process means, and then generating an A/D conversion command instructing performance of an A/D conversion according to said set order;

Shio JP '556 (about paragraphs [0004]-[0006]) discloses that arithmetics are performed by the DSP at timings of a timing signal CNT3 outputted from controller 10. But merely by starting to perform an arithmetic, the controller 10 of Shio does not teach or suggest "A/D conversion command means for first setting an order of acquiring digital signals outputted from the arithmetic process means, and then generating an A/D conversion command instructing performance of an A/D conversion according to said set order" as presently claimed by Applicants.

The additional citation of Imamura does not supply what is absent in Shio, as discussed above. The serial transfer means disclosed by Imamura does not teach or suggest a structure controlled on the basis of an instruction from an A/D conversion command means, as claimed by Applicants.

Thus, there is no disclosure or teaching in either of Shio or Imamura that would suggest Applicants' claimed invention to one of ordinary skill in the art. Further, there is no disclosure or teaching in either Shio or Imamura that would suggest the desirability of combining any portions thereof effectively to anticipate or suggest Applicants' presently claimed invention. Withdrawal of this rejection of claims 15 and 19 and allowance of same are therefore respectfully requested.

Accordingly, the application is now in condition for allowance and a notice to that effect is respectfully requested. The Commissioner is hereby authorized to charge/credit any fee

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deficiencies or overpayments to Deposit Account No. 19-4293 (Order No. 28951.1130). If a telephone conference could help place this application in even better condition for issue, the Examiner is invited to call Applicants' undersigned attorney at the number listed below.

Respectfully submitted,

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